

VeriSilicon | Asia Pacific

China's IP licensing leader enjoying synergy under SiPaaS model, Initiate OW

Stock rating

Over-weight

Target Price

RMB 92.38

Key Positive

Unique SiPaaS model creates a strong synergy to empower the one-stop chip customization service and IP business, maximizing the value of R&D achievements.

SiPaaS mode emphasizes taking independently developed semiconductor IP as the core to create a flexible and reusable chip design platform to provide customers with both one-stop chip customization services and IP licensing. The synergy under SiPaaS is shown as below: (1) Through providing the customization service, VeriSilicon can understand the IP market demand better and continuously enrich IP resource base; (2) High-quality IP will further attract customers to choose its chip customization service, realizing the mutual import of customers between businesses; (3) The self-owned IP resource base provides cost and design efficiency advantages in the one-stop customization business.

Running on the booming track, VeriSilicon's rich IP reserves and diversified customer base build higher barriers for potential competitors

VeriSilicon has a relatively complete IP pool composed of 6 types of processors IP and 1400+ digital-analog hybrid IP and RF IP, which gains it more expansion capability in diversifying the products' functions and applications to give customers a more comprehensive solution. Meanwhile, the increasing market recognition will drive the continuous optimization of operating performance. Especially when more and more well-known enterprises become its customers, such as Intel, Bosch, Amazon etc., VeriSilicon's brand competitiveness is further enhanced by providing a series of services with strong demonstration effect. **Given its domestic leading position in design IP, VeriSilicon is expected to fully enjoy the tailwind of China Design Market Expansions.**

Advantages of advanced nodes design capability and the scale effect of mass production appear, driving the rapid revenue growth of one-stop customization business

VeriSilicon's forward-looking strategic layout on the R&D earns the company advanced node design capability on CMOS, FinFET and FD-SOI. VeriSilicon already has successful taping experience of **28nm/22nm FD-SOI and 14nm/10nm/7nm/5nm FinFET and is currently promoting the iterative R&D of the Chiplets, the functional circuit blocks that can significantly shortens design time and cost of tape-out.** With the improvement of the proportion of the advanced process projects, the higher added value of the design service business can be expected. In 2021A, VeriSilicon's design service's revenue grew significantly by 104.5% yoy to RMB 548.5mn, with GM expanding from 8.2% to 10.1%. Given the much closer cooperation with different foundries, including SMIC, Gro Fonder, Samsung, TSMC, etc., the scale effect of mass production business is appearing, implied by a +35.4% yoy of chip production mgmt. business' revenue.

Global Equity Team

Arthur Tzeng

arthurtzengcuhkirs2022@gmail.com

Olivia Fu

oliviafucuhkirs2022@gmail.com

VeriSilicon (688521. CH)

Stock Rating	Over-weight
Target Price	RMB 92.4
Shr price (04/04/22)	RMB 48.6
Up/downside (%)	90%
52-Week Range	RMB104.87-47.7
Shares Out. (mn)	495.89
Mkt Cap (CNY bn)	RMB24.1bn
EV (CNY bn)	RMB22.4bn
Free Float (%)	41.4%

Fiscal year (12/31)

(CNY in mn)	2021A	2022E	2023E
Revenue	2,139.3	3,114.6	4,440.1
YoY (%)	42%	46%	43%
Gross Profit	857.1	1,306.4	1,924.9
GPM	40%	42%	43%
EBIT	20.0	230.3	570.6
OPM (%)	1%	7%	13%
Pre-Tax Income	24.2	237.0	577.3
Net Income	13.3	206.2	502.3
NPM	1%	7%	11%
Basic EPS	0.03	0.44	1.07

VeriSilicon | Asia Pacific

Key Positive (Cont.)

Verisilicon's transition from IP/IC Design Vendor to Chiplet Player

Based on the latest conference call of Verisilicon on March 30th ([link](#), 2022), the Chairman Wayne Dai mentioned its strong conviction to transit from a pure IP/IC Design player to **Chiplet players** – **Chiplet is a technique that could effectively bypass Moore's law by replacing a single silicon die with multiple smaller dice that work together in a unified package solution. The global market for processor microchips that utilize chiplets in their manufacturing process is set to expand to US \$5.8 billion in 2024. It said that this is rising from US \$645 million in 2018, reflecting a 44.2% CAGR from 18A-24E (Omidia, 2020).**

The Chairman also mention Chiplet could further shorten the R&D time and balance the efficiency and cost in advance progress (5nm/7nm). With China IC Design Company grow at 27% yoy to 2,810 players in total, it is believed that there are still big room for Verisilicon to acquire more customer base and IP revenue. We do recognize its aggressive moves in expanding R&D expenditure and solidify its market share by arranging 95% of R&D researcher in Mainland R&D center across Shanghai, Chengdu, Beijing, Nanjing (Offshore centers: US Silicon Valley, Dallas). On March 3rd. A broad range of industry stalwarts - Intel, AMD, Arm, TSMC, and Samsung, among others, introduced the new Universal **Chiplet Interconnect Express (UCIe)** with the goal of standardizing die-to-die interconnects between chiplets with an open-source design, thus reducing costs and fostering a broader ecosystem of validated chiplets. **On April 2nd, Verisilicon announce their new membership joining the Ucie – Marking the first China player join the alliance to develop Ucie 1.0 Standard and its applications for future Chiplet technology (link, 2022/4/2). As such, we hold a long-term positive convictions on its solid market power in China IP/IC Design/Chiplet segments, that China players can be involved in advance process despite the bottleneck of downstream fabless/foundries expansions.**

Initiate OW, with 12-month TP at 92.4 (90% upside)

We model Verisilicon's revenue at a +40.9% CAGR in 2022E-25E, reaching RMB 8.7bn revenue scale in 2025E, with 17.5% 25E NPM, yielding RMB 1.5bn net income and RMB 3.25 EPS. For valuation, we first adopt sum-of-the-part valuation to reach the TP at 92.4, with 25E based discounted PE multiple method yielding the similar valuation level. **Our TP implies a 14.71x 2022E PS and points to a total market value RMB45.8bn. Based on latest closing price on April 4th, there are 90% base case upsides to our TP, CUIRS initiate VeriSilicon OW.**

Key Negative Thesis

Slower-than-expected progress in IP R&D, portfolio expansion and monetization:

The industry is still under constant innovation, and there is uncertainty in R&D innovation, portfolio expansion and IP monetization. If the researched IP has no actual application value or the product expansion speed cannot keep up with the upstream and downstream markets, VeriSilicon is likely to lose its leading position, and the growth of IP business will also be limited.

Risk of foundry capacity tightness: Under the condition that the global foundry capacity is still tight, especially on advanced nodes, if VeriSilicon has a lower priority in capacity allocation or higher procurement cost among foundry suppliers, it'll have an adverse impact on the expansion of mass production business and profit margins.

Technology licensing risk: The company needs to obtain a technical license as required from third-party semiconductor IP and EDA tool suppliers which are mainly Synopsys and Cloudflare. If the company lack access to the advanced nodes due to **drastic changes in the international political and economic situation or other force majeure factors.**

VeriSilicon | Asia Pacific

Appendix

Verisilicon 2017A-2025E Financial Summary

Income Statement (RMB mn)

	2017A	2018A	2019A	2020A	2021A	2022E	2023E	2024E	2025E
Revenue	1,079.9	1,057.5	1,339.9	1,506.1	2,139.3	3,114.6	4,440.1	6,300.3	8,713.3
Cash COGS	(630.1)	(555.3)	(724.4)	(751.2)	(1,382.7)	(1,668.2)	(2,324.6)	(3,245.9)	(4,484.2)
COGS Depreciation & Amortization	(69.9)	(67.2)	(77.4)	(77.8)	(100.4)	(139.9)	(190.6)	(264.2)	(356.7)
Gross Profit	379.9	435.1	538.1	677.2	857.1	1,306.4	1,924.9	2,790.2	3,872.4
Other Operating Income	2.5	2.9	5.7	26.3	19.7	11.4	11.4	11.4	11.4
SG&A	(134.4)	(133.1)	(172.7)	(179.4)	(214.0)	(264.9)	(333.2)	(441.3)	(566.7)
R&D	(331.6)	(347.4)	(425.1)	(530.9)	(628.4)	(805.9)	(1,015.6)	(1,283.6)	(1,557.4)
D&A	(1.7)	(2.0)	(1.7)	(2.9)	(2.3)	(2.3)	(2.3)	(2.3)	(2.3)
Prov for Doubtful Asset	0.0	(2.5)	(0.2)	(0.9)	(10.0)	(10.0)	(10.0)	(10.0)	(10.0)
Other OPEX	(2.1)	(4.5)	(1.8)	(9.6)	(4.7)	(4.5)	(4.5)	(4.5)	(4.5)
Operating Income (Loss)	(87.4)	(51.5)	(57.6)	(17.3)	17.4	230.3	570.6	1,059.9	1,742.9
Non-Operating P&L	(33.4)	(7.1)	33.3	(5.2)	6.3	6.3	6.3	6.3	6.3
Pre-tax Income (Loss), Adjusted	(120.8)	(58.5)	(24.4)	(22.5)	23.7	236.6	576.9	1,066.2	1,749.2
Abnormal P&L	0.6	0.2	0.5	14.3	0.5	0.4	0.4	0.4	0.4
Pre-tax Income (Loss), GAAP	(120.2)	(58.3)	(23.9)	(8.2)	24.2	237.0	577.3	1,066.6	1,749.6
Tax Expense	(7.9)	(9.5)	(17.3)	(17.3)	(10.9)	(30.8)	(75.1)	(138.7)	(227.4)
Minority Interest	-	-	-	-	-	-	-	-	-
Net Income, GAAP	(128.1)	(67.8)	(41.2)	(25.6)	13.3	206.2	502.3	927.9	1,522.1
EBITDA	(87.4)	17.7	21.4	63.4	120.1	372.5	763.6	1,326.4	2,101.8
EPS (Basic, RMB)	(1.50)	(0.50)	(0.10)	(0.06)	0.03	0.44	1.07	1.98	3.25
EPS (Diluted, RMB)	(1.50)	(0.50)	(0.10)	(0.06)	0.03	0.44	1.07	1.98	3.25
Wtdavg Shares out. (basic) (mn)	85.4	136.4	398.5	468.6	468.6	468.6	468.6	468.6	468.6
Wtdavg Shares out. (diluted) (mn)	85.4	136.4	398.5	468.6	468.6	468.6	468.6	468.6	468.6

Growth & Margins (%)

Total revenue growth	N.A.	-2.1%	26.7%	12.4%	42.0%	45.6%	42.6%	41.9%	38.3%
EBITDA growth	N.A.	-120.2%	21.1%	195.9%	89.3%	210.3%	105.0%	73.7%	58.5%
EPS growth	N.A.	-66.7%	-80.0%	-40.0%	-147.3%	1451.4%	143.6%	84.7%	64.0%
Gross margin	35.2%	41.1%	40.2%	45.0%	40.1%	41.9%	43.4%	44.3%	44.4%
EBIT margin	-8.1%	-4.9%	-4.3%	-1.1%	0.8%	7.4%	12.9%	16.8%	20.0%
Net margin	-11.9%	-6.4%	-3.1%	-1.7%	0.6%	6.6%	11.3%	14.7%	17.5%

Verisilicon Peers in IP, design services — Key Financials

Metrics		Sales YoY			Gross Margin			EBIT Margin			Net Margin		
Forecast Year	Ticker	21A	22E	23E	21A	22E	23E	21A	22E	23E	21A	22E	23E
VERISILICON MI-A	688521 CH	42%	38%	33%	40%	41%	42%	1%	6%	9%	1%	5%	7%
CEVA INC	CEVA US	22%	17%	12%	86%	83%	83%	3%	18%	19%	12%	14%	15%
SYNOPTICS INC	SNPS US	20%	10%	13%	81%	81%	82%	20%	30%	34%	27%	25%	27%
CADENCE DESIGN	CDNS US	11%	12%	10%	91%	91%	91%	26%	38%	40%	31%	31%	33%
EMEMORY TECH	3529 TT	33%	35%	14%	100%	100%	100%	54%	61%	68%	47%	53%	55%
ALPHAWAVE IP	AWE LN	110%	81%	37%	96%	96%	95%	58%	65%	58%	43%	44%	44%
CAMBRICON-A	688256 CH	55%	40%	40%	54%	55%	53%	-124%	-92%	-53%	-123%	-91%	-48%
AVG		42%	33%	21%	85%	84%	84%	32%	42%	43%	32%	33%	35%
GLOBAL UNICHIP	3443 TT	11%	21%	16%	35%	34%	34%	11%	12%	13%	10%	10%	11%
ALCHIP TECH	3661 TT	47%	40%	41%	34%	34%	33%	18%	19%	19%	14%	15%	16%
BESTECHNIC SHA-A	688608 CH	71%	59%	44%	37%	39%	39%	23%	24%	23%	23%	23%	24%
AMLOGIC SHANGH-A	688099 CH	74%	37%	26%	38%	38%	38%	17%	18%	18%	17%	17%	18%
AVG		51%	39%	32%	36%	36%	36%	17%	18%	18%	16%	17%	17%

Verisilicon Peers in IP, design services — Multiples (x)

Metrics		P/S			EV/Sales			EV/EBIT			P/E		
Forecast Year	Ticker	21A	22E	23E	21A	22E	23E	21A	22E	23E	21A	22E	23E
VERISILICON MI-A	6533 TT	11.9x	8.7x	6.5x	11.2x	8.1x	6.1x	1153.6x	141.2x	70.5x	1302.3x	163.3x	87.4x
CEVA INC	CEVA US	7.9x	6.7x	6.0x	6.7x	5.7x	5.1x	97.4x	64.7x	54.6x	63.1x	48.8x	39.8x
SYNOPTICS INC	SNPS US	11.9x	10.8x	9.5x	11.7x	10.7x	9.4x	27.3x	23.0x	18.0x	44.7x	42.5x	34.8x
CADENCE DESIGN	CDNS US	15.5x	13.8x	12.5x	15.3x	13.6x	12.3x	46.5x	23.3x	19.1x	50.3x	44.0x	38.4x
EMEMORY TECH	3529 TT	60.2x	44.6x	39.3x	59.2x	43.9x	38.6x	27.0x	21.4x	18.0x	129.3x	84.6x	71.9x
ALPHAWAVE IP	AWE LN	16.4x	9.1x	6.6x	10.9x	6.0x	4.4x	353.7x	110.0x	62.3x	38.2x	20.6x	15.1x
CAMBRICON-A	688256 CH	36.0x	25.6x	18.3x	30.8x	21.9x	15.7x	-24.3x	-23.3x	-37.3x	-29.2x	-28.1x	-37.9x
AVG		24.6x	18.4x	15.4x	22.4x	17.0x	14.2x	102.7x	46.9x	32.6x	65.1x	48.1x	40.0x
GLOBAL UNICHIP	3443 TT	4.6x	3.8x	3.3x	4.1x	3.4x	2.9x	37.0x	28.7x	22.8x	47.5x	37.1x	30.1x
ALCHIP TECH	3661 TT	7.4x	5.3x	3.8x	6.7x	4.7x	3.4x	38.0x	25.1x	17.5x	52.1x	34.5x	23.3x
BESTECHNIC SHA-A	688608 CH	11.8x	7.4x	5.2x	8.9x	5.6x	3.9x	38.1x	23.8x	16.8x	51.5x	31.8x	21.9x
AMLOGIC SHANGH-A	688099 CH	9.9x	7.2x	5.7x	9.3x	6.8x	5.4x	54.3x	38.6x	29.6x	58.6x	41.4x	31.6x
AVG		8.4x	5.9x	4.5x	7.3x	5.1x	3.9x	41.9x	29.1x	21.7x	52.5x	36.2x	26.7x

VeriSilicon | Asia Pacific

Appendix

Revenue Breakdown & GP Mix

	2017A	2018A	2019A	2020A	2021A	2022E	2023E	2024E	2025E
Revenue Mix (RMB mn)	1,079.9	1,057.5	1,339.9	1,506.1	2,139.3	3,114.6	4,440.1	6,300.3	8,713.3
One-stop custom chip service	800.0	745.9	902.2	921.6	1,433.2	2,074.5	2,963.5	4,247.1	5,854.9
Chip production mgmt. services	589.5	439.6	533.4	653.4	884.7	1,165.1	1,572.8	2,123.4	2,866.6
Chip design services	210.5	306.4	368.8	268.2	548.5	909.5	1,390.6	2,123.7	2,988.3
IP licensing service	279.9	311.6	437.7	584.5	706.1	1,040.1	1,476.7	2,053.2	2,858.4
IP license	200.3	214.1	343.0	504.0	609.8	909.6	1,310.4	1,823.8	2,518.1
IP royalty	79.6	97.5	94.7	80.5	96.3	130.5	166.3	229.3	340.3
Revenue YoY	n.a.	-2.1%	26.7%	12.4%	42.0%	45.6%	42.6%	41.9%	38.3%
One-stop custom chip service	n.a.	-6.8%	20.9%	2.2%	55.5%	44.7%	42.9%	43.3%	37.9%
Chip production mgmt. services	n.a.	-25.4%	21.3%	22.5%	35.4%	31.7%	35.0%	35.0%	35.0%
Chip design services	n.a.	45.5%	20.4%	-27.3%	104.5%	65.8%	52.9%	52.7%	40.7%
IP licensing service	n.a.	11.3%	40.5%	33.5%	20.8%	47.3%	42.0%	39.0%	39.2%
IP license	n.a.	6.9%	60.2%	46.9%	21.0%	49.2%	44.1%	39.2%	38.1%
IP royalty	n.a.	22.5%	-2.9%	-15.0%	19.6%	35.5%	27.4%	37.9%	48.4%
Revenue Contribution	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
One-stop custom chip service	74.1%	70.5%	67.3%	61.2%	67.0%	66.6%	66.7%	67.4%	67.2%
Chip production mgmt. services	54.6%	41.6%	39.8%	43.4%	41.4%	37.4%	35.4%	33.7%	32.9%
Chip design services	19.5%	29.0%	27.5%	17.8%	25.6%	29.2%	31.3%	33.7%	34.3%
IP licensing service	25.9%	29.5%	32.7%	38.8%	33.0%	33.4%	33.3%	32.6%	32.8%
IP license	18.5%	20.2%	25.6%	33.5%	28.5%	29.2%	29.5%	28.9%	28.9%
IP royalty	7.4%	9.2%	7.1%	5.3%	4.5%	4.2%	3.7%	3.6%	3.9%

Exhibit 2: GPM Forecasts by segments

	2017A	2018A	2019A	2020A	2021A	2022E	2023E	2024E	2025E
Gross Profit Margin	35.18%	41.14%	40.16%	44.96%	40.06%	41.95%	43.35%	44.29%	44.44%
One-stop custom chip service	15.1%	18.1%	13.7%	7.8%	9.0%	10.0%	11.6%	13.1%	13.1%
Chip production mgmt. services	16.4%	18.4%	11.6%	14.5%	15.4%	17.4%	19.4%	21.0%	21.0%
Chip design services	11.34%	17.58%	16.72%	8.20%	10.1%	12%	15%	18%	18%
IP licensing service	92.7%	96.4%	94.8%	95.9%	94.2%	95.6%	95.6%	95.6%	95.6%
IP license	89.8%	94.7%	93.3%	95.2%	93.3%	95.0%	95.0%	95.0%	95.0%
IP royalty	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
Gross Profit Contribution	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
One-stop custom chip service	74.1%	70.5%	67.3%	61.2%	22.37%	23.87%	26.69%	29.68%	29.44%
Chip production mgmt. services	54.6%	41.6%	39.8%	43.4%	15.90%	15.52%	15.85%	15.98%	15.55%
Chip design services	19.5%	29.0%	27.5%	17.8%	6.47%	8.35%	10.84%	13.70%	13.89%
IP licensing service	25.9%	29.5%	32.7%	38.8%	77.63%	76.13%	73.31%	70.32%	70.56%
IP license	18.5%	20.2%	25.6%	33.5%	66.40%	66.14%	64.67%	62.10%	61.78%
IP royalty	7.4%	9.2%	7.1%	5.3%	11.23%	9.99%	8.64%	8.22%	8.79%

Exhibit 18 : Management Profile

Name	Position	Experience
Wei-Ming Dai/ Wayne	CEO	Mr. Wayne is an American citizen who holds a PhD in Electronic Computing Engineering from the University of California, Berkeley. Mr. Wayne was a professor at the University of California, Santa Cruz, Chairman and President of Utima, and Co-Chairman and Chief Technology Officer of Synod. He has published more than 100 papers in various technical journals and conferences, won the honorary title of "Top Ten Entrepreneurship" in China in 2005, and currently serves as Vice Chairman of the Global Innovation Center. Mr. Wayne has profound professional knowledge and rich experience in business management.
Wei-Jin Dai	Director, Vice President	Mr. Dai is an American citizen who holds a master's degree in electronic computing engineering from the University of California, Berkeley. Mr. Dai joined VeriSilicon from 2016 and is currently a director and vice president of VeriSilicon. Prior to joining VeriSilicon, Mr. Dai served as President and CEO of Picture Core USA, Vice President of Encounter product line of Cadence Design Systems's leading Digital implementation Systems Division, and Vice President of Silicon Perspective Corporation R&D department.
Wen-xi Shi	CFO	Ms. Shi is a Chinese national who holds a bachelor's degree and is a Certified Public Accountant in China, a Chartered Accountant in the United Kingdom, a Certified Public Accountant in Hong Kong and a Certified Public Accountant in the United States of America. Ms. Shi has served as Chief Financial Officer of VeriSilicon since she joined in 2006. Prior to joining VeriSilicon, Ms. Shi served as Chief Financial Officer of Phil Chuangna Special Fiber products Co., Ltd., Financial Analysis Manager of Huapu Information Technology Co., Ltd., and auditor of Ernst & Young.

For the full version of the report including financial forecast, valuation, company and industry summary, please comment on our LinkedIn post with your email address.

We are happy to share CUIRS insight with you!